AMENDMENTS TO THE CLAIMS

1. (Previously presented) A circuit comprising:

a surge suppressing circuit comprising:

a diode connected with an input of the surge suppressing circuit, and

first and second transistors which are arranged as a complementary Darlington pair that is connected in series between the diode and an output of the surge suppressing circuit.

2. (Currently amended) A circuit ~~as set forth in claim 1, further~~ comprising:

a surge suppressing circuit comprising:

a diode connected with an input of the surge suppressing circuit,

first and second transistors which are arranged as a complementary Darlington pair that is connected in series between the diode and an output of the surge suppressing circuit;

a resistor connected between the emitter of the first transistor and the base of the second transistor; and

a Zener diode connected between the base of the second transistor and ground.

3. (Currently amended) A circuit as set forth in claim 1, wherein the first transistor is a PNP type transistor and wherein the second transistor is a NPN type transistor.

4. (Previously presented) A circuit as set forth in claim 1, wherein the collector of the second transistor is connected to the base of the first transistor.

5. (Previously presented) A circuit as set forth in claim 2, further comprising a diode which is electrically connected with the emitter of the first transistor.

6. (Original) A circuit as set forth in claim 2, wherein the resistor is connected to a junction between the diode and the emitter of the first transistor.

7. (Previously presented) A circuit as set forth in claim 2, further comprising a capacitor connected between ground and the base of the second transistor and in parallel with the Zener diode.

8. (Previously presented) A method of surge suppression comprising:
connecting a diode with an input of a surge suppression circuit, and
interposing a complementary Darlington pair between the diode and an output of the surge suppressing circuit.

9. (Currently amended) A method as set forth in claim 8, wherein the complementary Darlington pair is configured by:
using a PNP transistor as the first transistor;
using a NPN transistor as the second transistor; and
connecting the base of the first transistor to the collector of the second transistor.

10. (Original) A method as set forth in claim 9, further comprising:
arranging a resistor between the input and a base of the second transistor; and
connecting the base of the second transistor to ground via a Zener diode.

11. (Previously presented) A method as set forth in claim 8, further comprising connecting a resistor between the diode and a base of one of the complementary Darlington pair of transistors.

12. (Previously presented) A method as set forth in claim 8, further comprising connecting a Zener diode between ground and the base of the one of the complementary Darlington pair of transistors.

13. (Previously presented) A method as set forth in claim 8, further comprising connecting a Zener diode connected in series with a resistor between the diode and ground.

14. (Previously presented) A method as set forth in claim 13, further comprising connecting a base of a one of the complementary Darlington pair to the Zener diode.

15. (Previously presented) A method as set forth in claim 11, wherein the one of the complementary Darlington pair of transistors is a NPN type transistor.